THE UNIVERSITY OF ALBERTA

FERRITE CORE MEMORY

by

STACEY D. JARVIN

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The undersigned certify that they have read, and recommended to the Faculty of Graduate Studies for acceptance, a thesis entitled Ferrite Core Memory, submitted by Stacey D. Jarvin in partial fulfillment of the requirements for the degree of Master of Science.

ABSTRACT

This thesis deals with the design of a ferrite core memory and the associated circuitry to cause information which has been written in to be read out after a desired time interval.

A unijunction transistor oscillator and flip flop divider system produces clock pulses over a wide range of frequencies to set the time delay desired. Information is written in, twelve bits in parallel in the form of a binary word, for 100 words serially. The first word that was written is then read out just before new information is written in the same set of cores. Thereafter, the sequence of reading out just before writing in continues. The time delay, then, is the time required to write in 100 words. The outputs from the cores are amplified and fed to holding flip flops.

The unit also supplies the clock pulses required to initiate an analog to digital conversion, and the clock pulses required for a digital to analog converter.

The complete system of analog to digital conversion, storage for a set time, and digital to analog conversion will provide a pure time delay of a voltage function, which is necessary in many analog computer problems.

ACKNOWLEDGEMENTS

The writer wishes to express his appreciation for assistance received during the preparation of this work. The project described in this thesis was carried out at the University of Alberta under the supervision of Y. J. Kingma, to whom the writer wishes to acknowledge his indebtness for assistance and advice throughout.

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INTRODUCTION

In analog computer work, particularly in the simulation of physical systems, there is often a need for a pure time delay. This requires that a voltage be reproduced in shape, but delayed in time. Several schemes are possible, [1] however the one that has been chosen consists of an analog to digital conversion, a storage, and a digital to analog conversion after the desired delay. The analog to digital encoder is under construction, and the digital to analog decoder has already been built. This project is concerned with the storage of the digital information, the readout after the desired delay, and the production of the required clock pulses for the other two units.

The analog to digital converter being built will produce a binary number of ten digits plus a sign bit, so that eleven binary bits of information must be stored for each sample of the analog signal taken. If 100 samples are to be stored in the delay interval, eleven planes of 100 cores each are necessary for the storage. After the 100 samples have been taken the information is read out of the first set of cores just before new information is to be written in. Thus the delay is slightly more than 100 times the

clock period, the extra being due to storage and read-out times in the memory. The minimum clock period is the analog to digital encoding time, plus storage times. The time for this conversion is 20 microseconds. If the maximum resolution of 100 samples is to be used in the delay interval, the minimum delay is approximately two milliseconds, which is adequate for use with the Pace analog computer. Shorter delay intervals might be obtained by taking fewer samples in the delay interval, i.e., by starting the readout before all the cores are full. This would, of course, lead to less accuracy in the reconstructed signal than if all the cores were used.

MAGNETIC CORE OPERATION[2]

Magnetic cores act as a memory by virtue of the fact that they can be left in two states of remnant magnetization, as shown in Figure 1. These two states

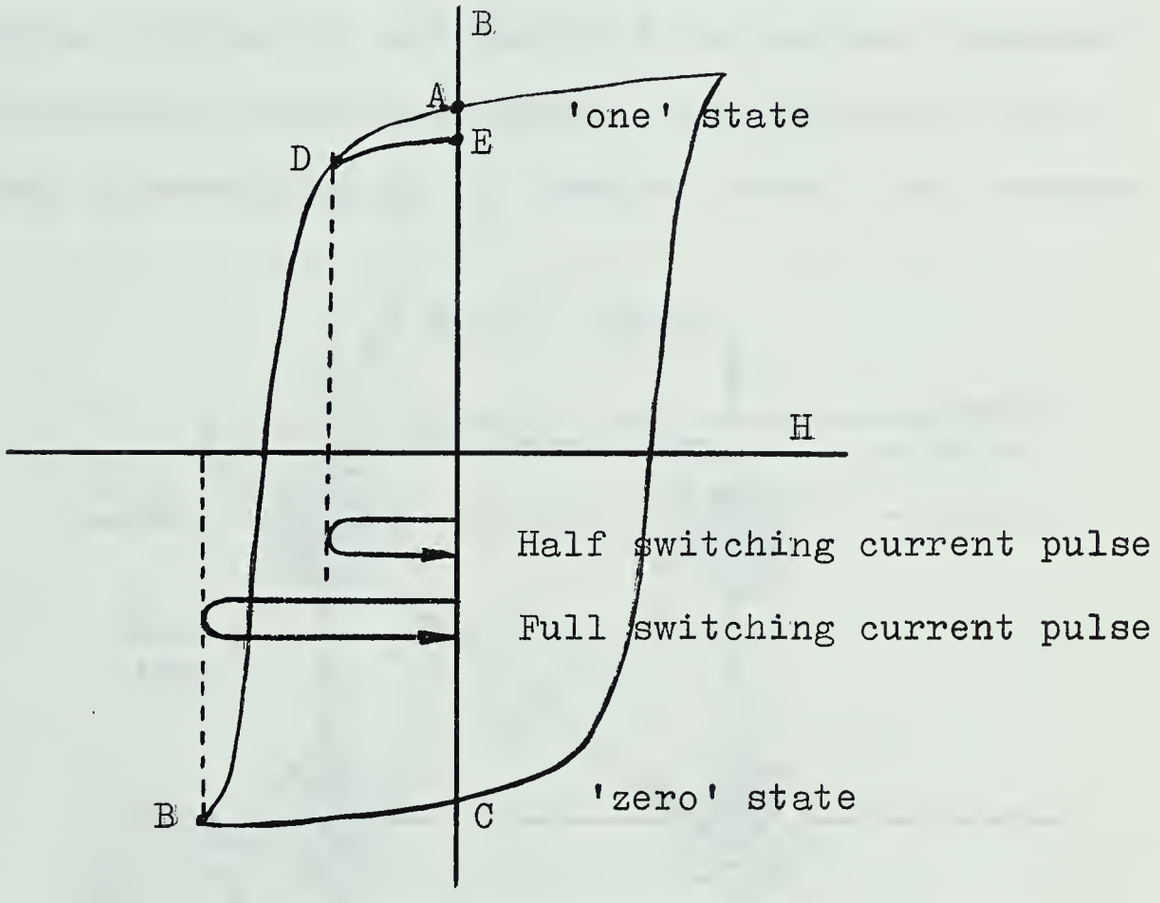


FIGURE 1 B-H CURVE FOR A FERRITE CORE

may be arbitrarily represented by a binary 'one' or 'zero', hence each core can store one binary digit or 'bit', Magnetizing fields of sufficient magnitude to induce magnetization are produced by passing electric currents, usually pulses, through turns around

the core, or more commonly, through a single turn consisting of a wire through the center of the toroid. The two states of magnetization are obtained by passing current in opposite directions through the same wire. To make addressing simpler for a large number of cores, they are threaded in a matrix fashion (Figure 2) and one half the current necessary for switching states is passed through each of the wires intersecting at the desired core. The currents

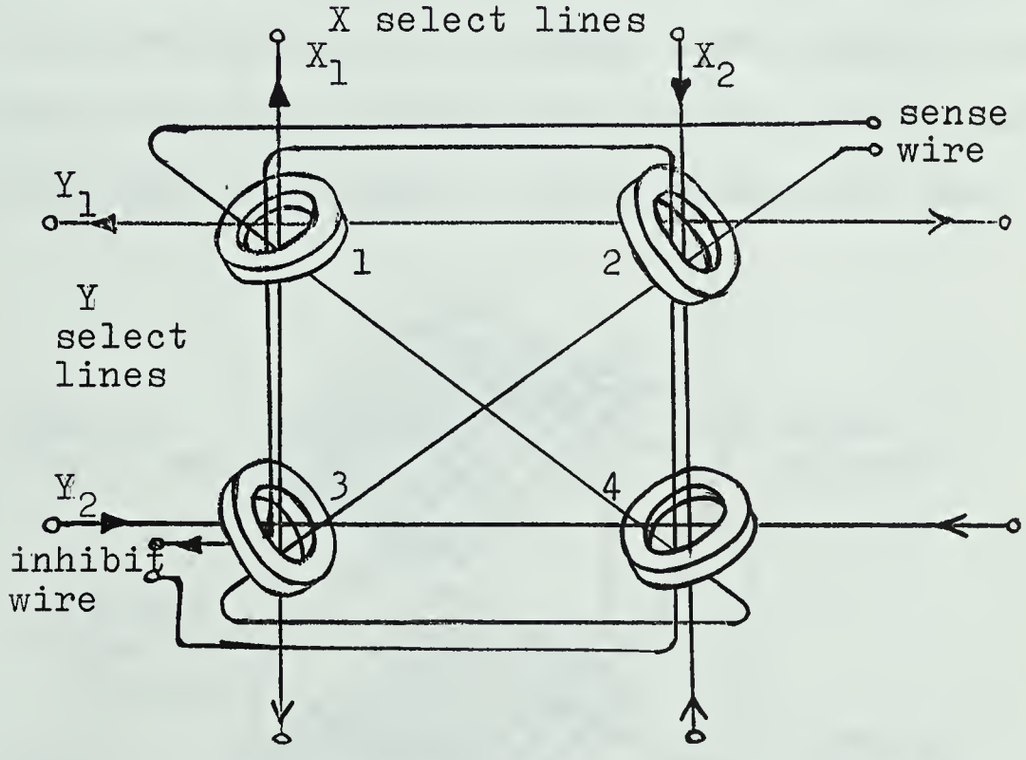


FIGURE 2 WIRING OF A TYPICAL MATRIX PLANE

add at the addressed core and produce a sufficient magnetic field to switch it. The half currents also

flow through several other cores, but if the core material has a fairly square hysteresis loop, they will not switch. The mechanics of this, shown in Figure 1, are as follows. The full switching current pulse will change the magnetization from A to B to rest at C and the state will have been changed. The half current pulse will take the magnetization from A to D to E and the state is essentially unchanged. It is, however, slightly disturbed.

When it is desired to write in more than one 'bit' in parallel, i.e., a binary word, several planes are connected using common drive wires, into a core stack as shown in Figure 3. This eliminates the

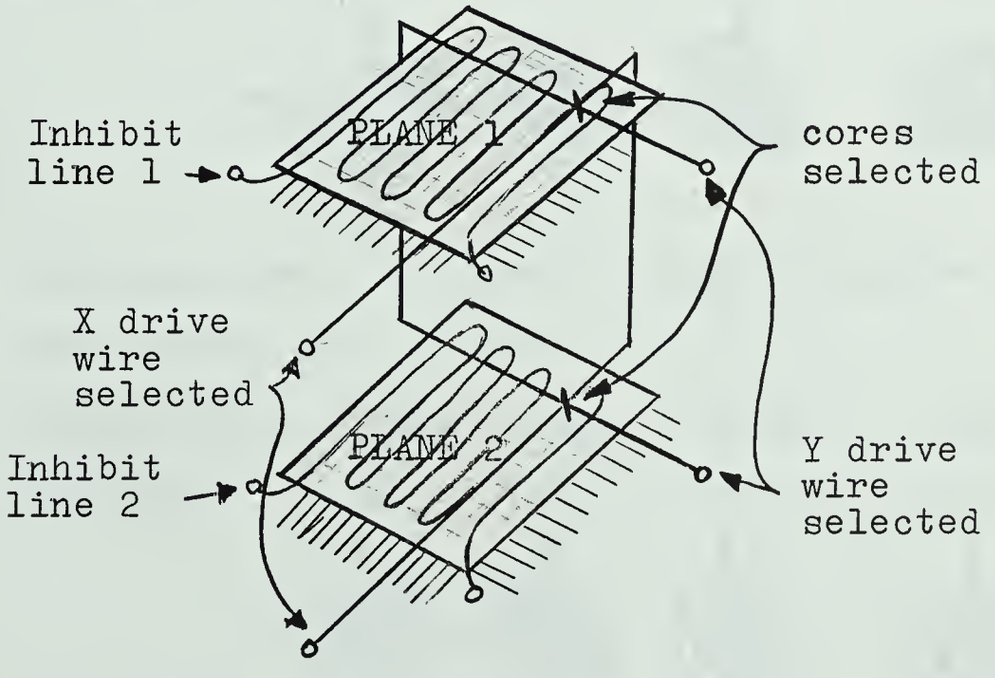
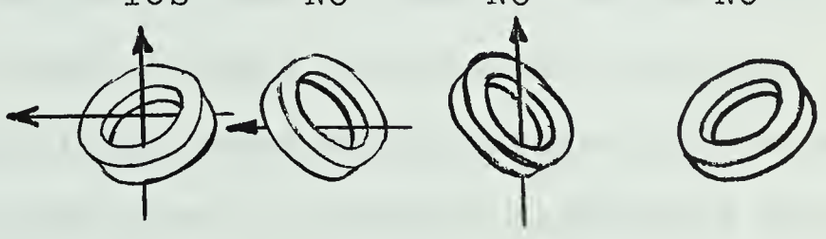


FIGURE 3 TWO PLANE CORE STACK WITH INHIBIT AND DRIVE WIRES SHOWN

need for additional selection circuits for each plane. Since combinations of 'ones' and 'zeros' are to be written in, and a common drive pulse would write in all 'ones', switching must be prevented at the cores where a 'zero' is to be written. An 'inhibit wire' is threaded through the cores in each plane of the stack, as shown in Figures 2 and 3. Through this is driven a half amplitude current pulse identical to the select current pulses. This extra current is

A. Writing a 'one' in core 1 (no inhibit current)

core number	1	2	3	4
net current through core	Full	Half	Half	None
switched?	Yes	No	No	No



B. Writing a 'zero' in core 1 (inhibit current flowing)

core number	1	2	3	4
net current through core	Half	None	None	Half
switched?	No	No	No	No

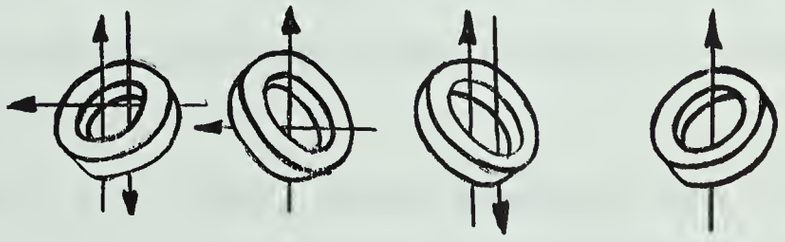


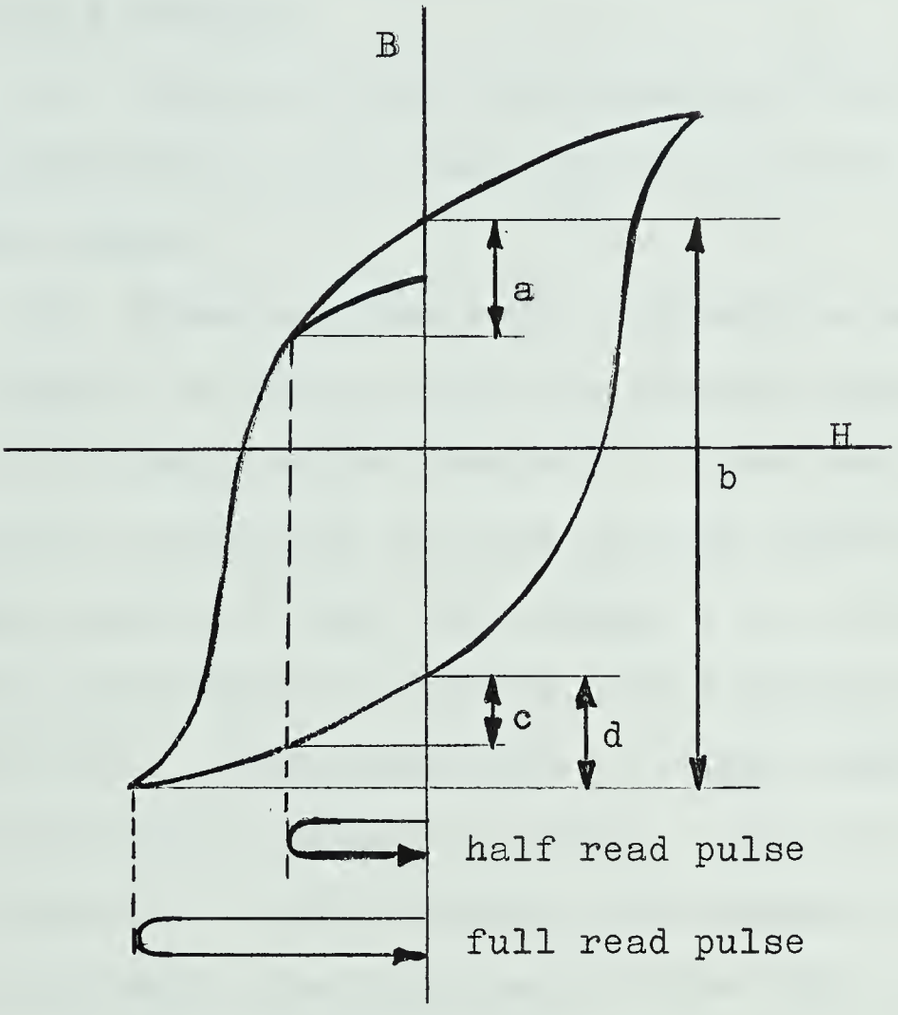
FIGURE 4 CURRENTS DURING WRITING OF THE CORES OF FIGURE 2

such that it opposes half of the select current through the selected core and so prevents it from switching. This inhibit current is withheld when a written 'one' is desired, and the core is allowed to switch. This procedure is shown diagrammatically in Figure 4.

Readout is accomplished by driving the selected core to the zero state by pulses on the select wires in the opposite direction to writing. The inhibit wires are not used. If the core was in the 'one' state it will switch and the change in flux (Figure5) will be picked up as a small voltage pulse by the sense wire which is threaded diagonally through the cores in each plane as in Figure 2. A core which is in the 'zero' state and hence does not switch, produces only a small output. Small outputs will also be obtained from all the cores which receive half read pulses. The sense wire is threaded diagonally through the cores in such a fashion as to minimize the pickup from those that are disturbed. This cross threading also reduces pickup on the sense wire from current pulses on the drive wires. This type of threading results in the output being voltage pulses of either polarity.

The fact that all cores, after reading, are in the 'zero' state makes it unnecessary to set them to

'zero' for the next write cycle, as is needed for the inhibit system of switching.



a - Flux change from a 'one', half read
b - Flux change from a 'one', fully read
c - Flux change from a 'zero', half read
d - Flux change from a 'zero', fully read

FIGURE 5 B-H CURVE SHOWING FLUX CHANGES FROM SWITCHING PULSES OF FULL AND HALF AMPLITUDE

BASIC DESIGN CONSIDERATIONS

The power supplies were chosen as plus and minus six volts because:

(1) These were the requirements of the Philips logic building blocks which were to be used for most of the system.

(2) These supplies were available as part of the digital to analog converter already constructed.

(3) They would be adequate for the core switches.

To be compatible with the Philips building block system, negative logic was chosen, i.e., a binary 'zero' corresponds to 0 volts, and a binary 'one' to -6 volts. This means that all logic operations are performed on negative signals. All flip flops and monostable multivibrators are triggered on the positive going (trailing) edge of the logic pulse. However, core switching was chosen to take place on the negative going (leading) edges of the logic pulses so that outputs would occur within the strobing pulses. It was desirable to perform all logic with strobing pulses (shorter, delayed pulses which essentially sample the logic) rather than just using the logic levels directly, even though it adds somewhat to the cost because:

(1) At longer delay times, there are long resting periods between switching, and with normal logic the switches would be on and drawing full currents during this period. This would result in a considerable extra power drain, and unnecessary heating of components. Under strobing conditions, full switching currents are drawn for only four microseconds in each cycle, or one fifth of the period at the maximum repetition rate, hence components can be overrated for intermittent duty.

(2) The Philips flip flops are quite slow, and take about 3 microseconds to reach their logic voltages when loaded. This is not a fast enough waveform for core switching, but a faster and slightly delayed strobing pulse speeds up the logic greatly.

(3) With the inhibit system of switching, it is important that the switching currents be identical in time. Strobing the switches with the same strobing pulse ensures this.

COMPLETE SYSTEM

The block diagram of the complete system is shown in Figure 6 and the relationships of the pulses in it, in Figure 7.

The time base oscillator is a unijunction transistor oscillator with variable timing elements to produce variable frequency timing pulses from 2 kc. to 50 kc. A divide by 100 flip flop counter allows a further reduction in frequency if desired, providing delays of 2 msec. to 50 seconds. These timing pulses are fed to a squaring inverter, which ensures a fast negative going voltage to initiate the analog to digital conversion. This squaring amplifier also feeds an isolation amplifier which triggers a monostable multivibrator with a period sufficient to allow the analog to digital conversion to be made before the writing takes place. This monostable multivibrator triggers the write control which consists of fout flip flops connected to count by ten. The outputs of these flip flops are selected by seven gates in such a way that their outputs, taken in pairs, will select any one of the ten core lines. Since the outputs of the flip flops and gates are not fast enough to drive the core switches, the

input to the write control is also used to trigger two monostable multivibrators in series. The second of these produces a fast narrow strobing pulse after a short delay. This strobing pulse is used in conjunction with the gated outputs of the flip flops to produce shorter, sharper, and more uniform switching pulses, regardless of the stepping rate of the control. Each pulse into the control selects the next line along the side of the core matrix, the X coordinate. A gate selects the signal which drives the tenth core line and steps the Y control one step. The Y control is similiar to the X, in that it uses four flip flops, selected by seven gates connected in the same fashion. Its gates, however, are driven with the strobing pulse from the X control, so that the switching pulses occur on the X and Y lines at the same time. Because the Y steps less often, ten clock pulses pass through its gates for each logic state, rather than one as in the X. In this fashion the 100 cores in the matrix are selected sequentially.

A gate selects the pulse which switches the 99th core and uses it to set a flip flop to the one state. The output from this flip flop opens a gate which allows the strobing pulses from the write control

to step the read control. The read control is identical in construction and operation to the write control, except that it acts 99 steps and a few microseconds behind the write control. This makes up the desired delay.

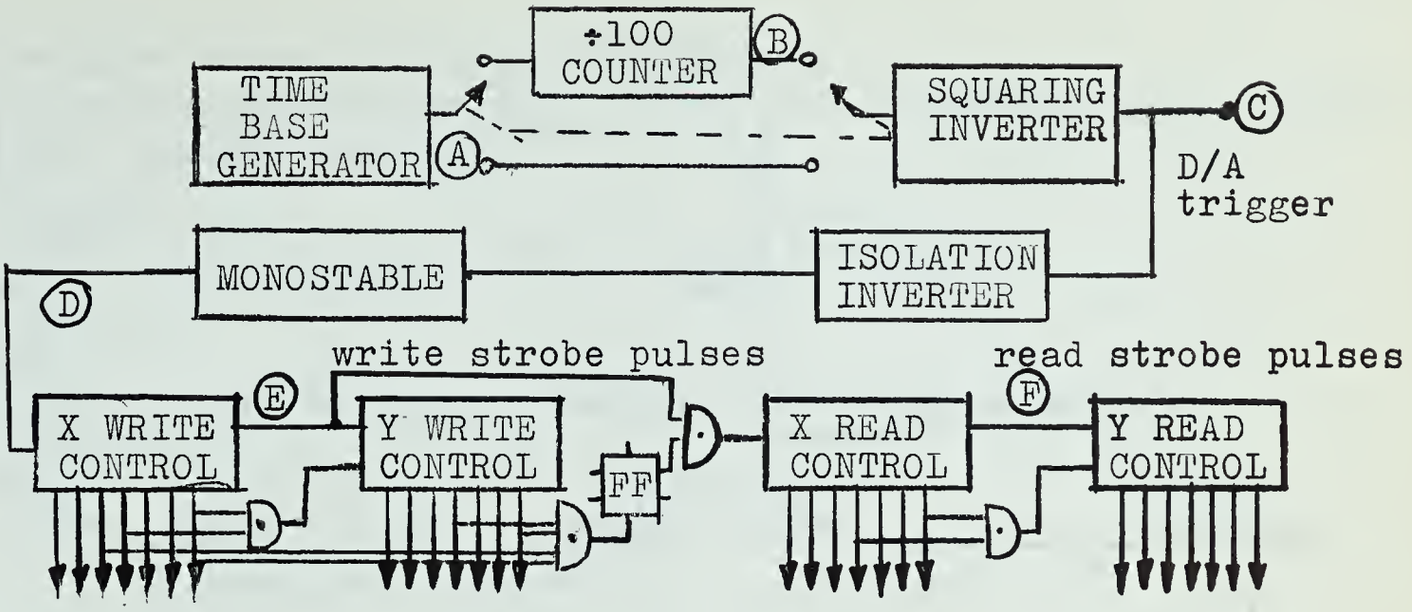
The outputs from the control unit gates are distributed among switches on both ends of the core lines. These switches are arranged in groups such that the seven switches, driven with the proper pulses, can select any one of the ten control lines, and the complete set of switches can drive read or write currents through any one of the 100 cores in each plane.

The digit inhibit switches are driven directly from the analog to digital converter outputs. The inputs are also gated with the write strobe pulse so that inhibit current is only driven through the matrix when select current is flowing.

The readout amplifiers change the small bidirectional pulses from the cores into unidirectional switching pulses and remove the unwanted outputs resulting from the write cycle and from switching noise. The output pulses are used to set holding flip flops. These flip flops are reset by the following write pulse in preparation for the next read

cycle.

Clock pulses for the digital to analog converter must be both positive and negative going five volt pulses, and occur within the readout pulse. Since the readout is held by a flip flop, this inclusion requirement is not too hard to meet. A monostable multivibrator driven from the write control strobing pulse is adjusted so that it switches just after the flip flops have been set and have reached their logic voltages. The output from the monostable multivibrator is differentiated, and the resulting spike amplified to a switching pulse for the negative clock pulse required. Another amplifier yields the positive switching pulse.



control outputs to X and Y core line read and write switches

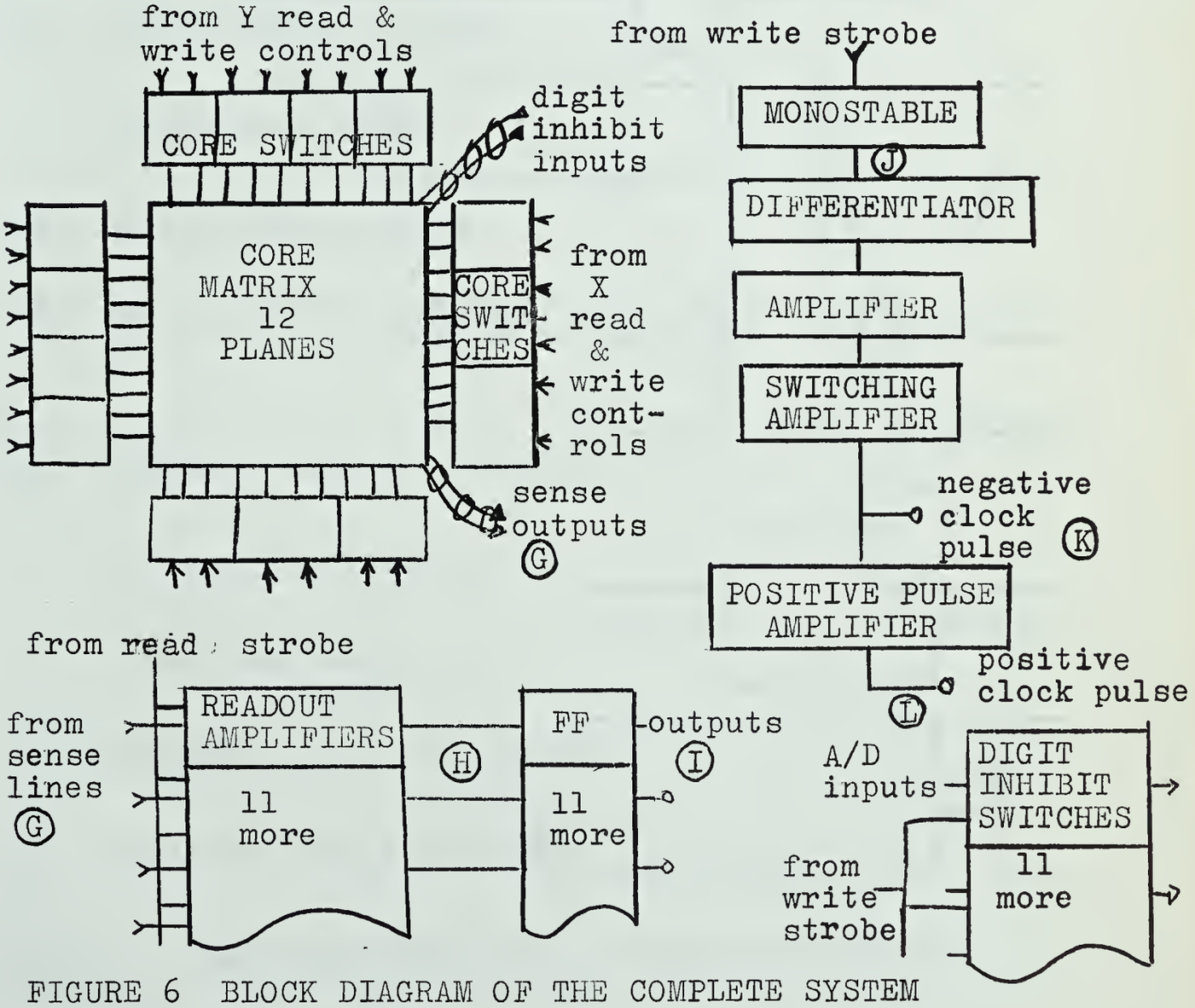


FIGURE 6 BLOCK DIAGRAM OF THE COMPLETE SYSTEM

Letters refer to points on Figure 6.

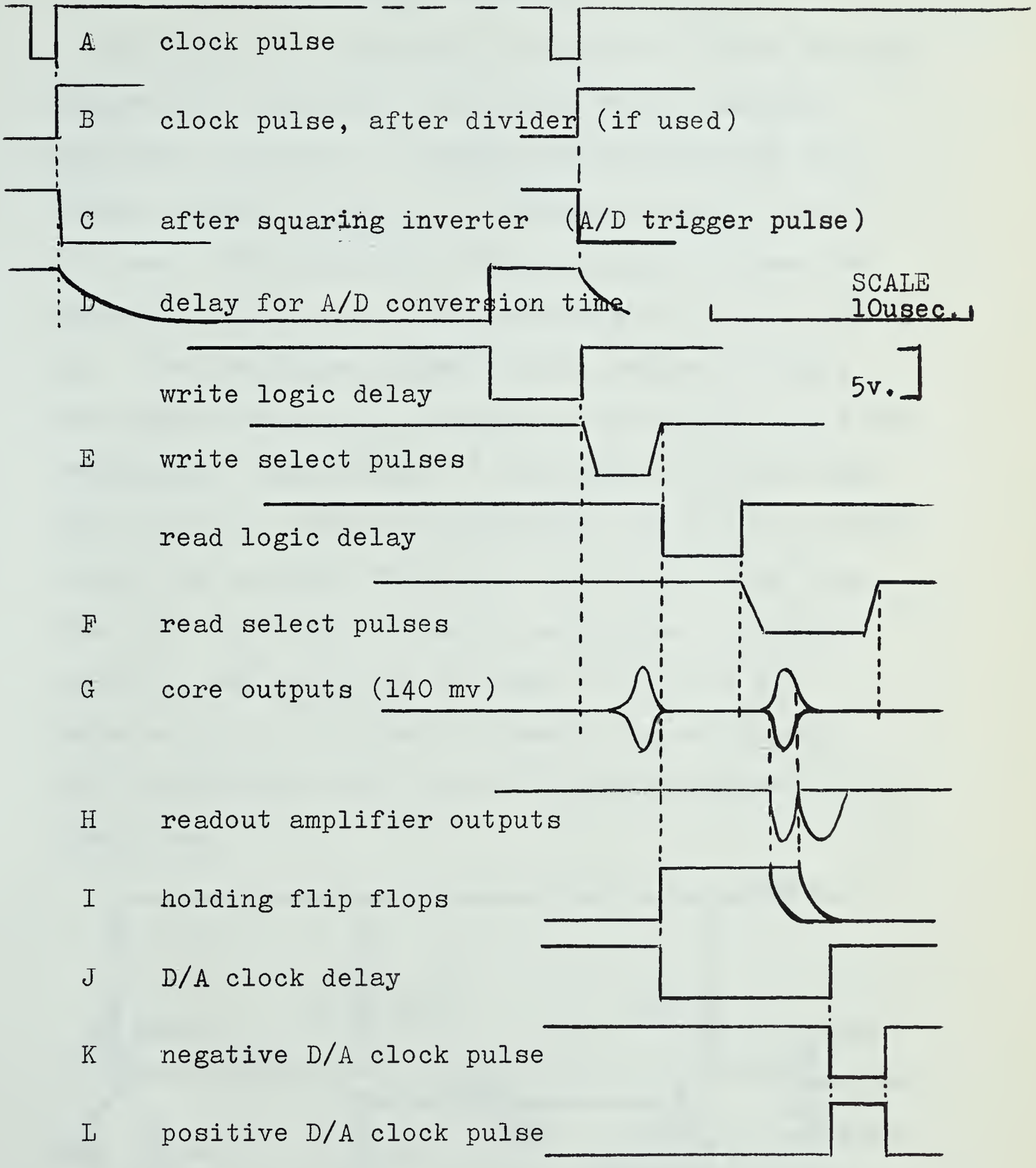


FIGURE 7 TIME RELATIONSHIPS OF PULSES IN FIGURE 6

TIME BASE GENERATOR

The time base generator consists of a free running unijunction transistor oscillator with a maximum frequency of 50 kcs. Varying the resistance in the timing circuit adjusts the frequency from 50 kcs. to 6.5 kcs. Switching the timing capacitor allows the adjustment to be made over the range 7.2 kcs to 200 cps. Used with the divide by 100 counter circuit, the output frequency is variable from 50 kcs. to 2 cps. Temperature compensation [3] by means of R_2 has been used. Over the expected temperature range to be encountered, the expected frequency variation [3] is less than ½%. The output from the oscillator is sensed across R_1 and amplified to about 8 volts by T_2. Resistor R_3 is included to prevent the oscillator from locking out when the poteniometer resistance is turned out.

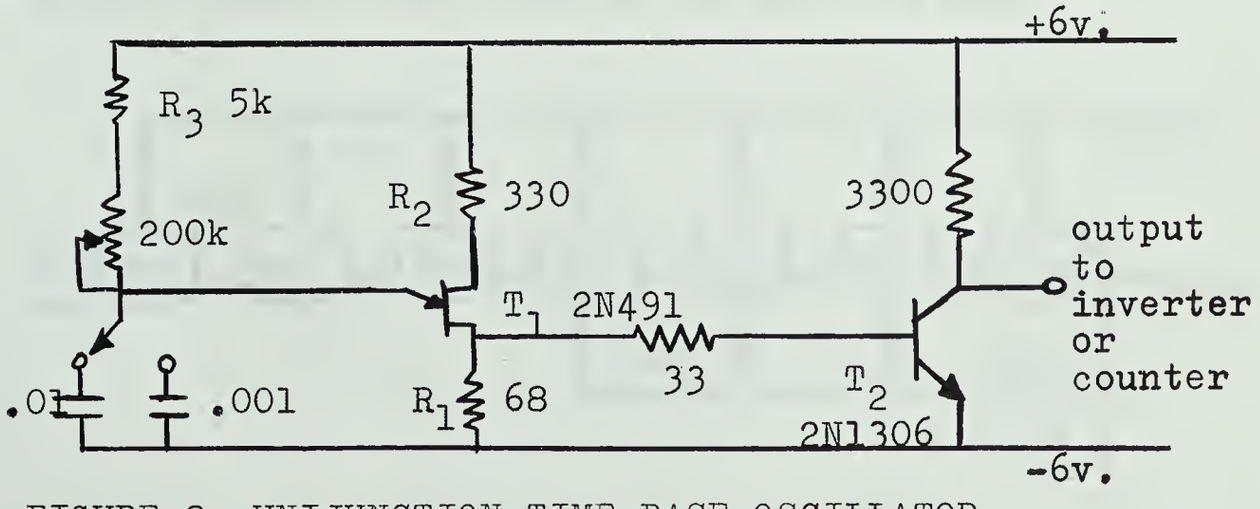


FIGURE 8 UNIJUNCTION TIME BASE OSCILLATOR

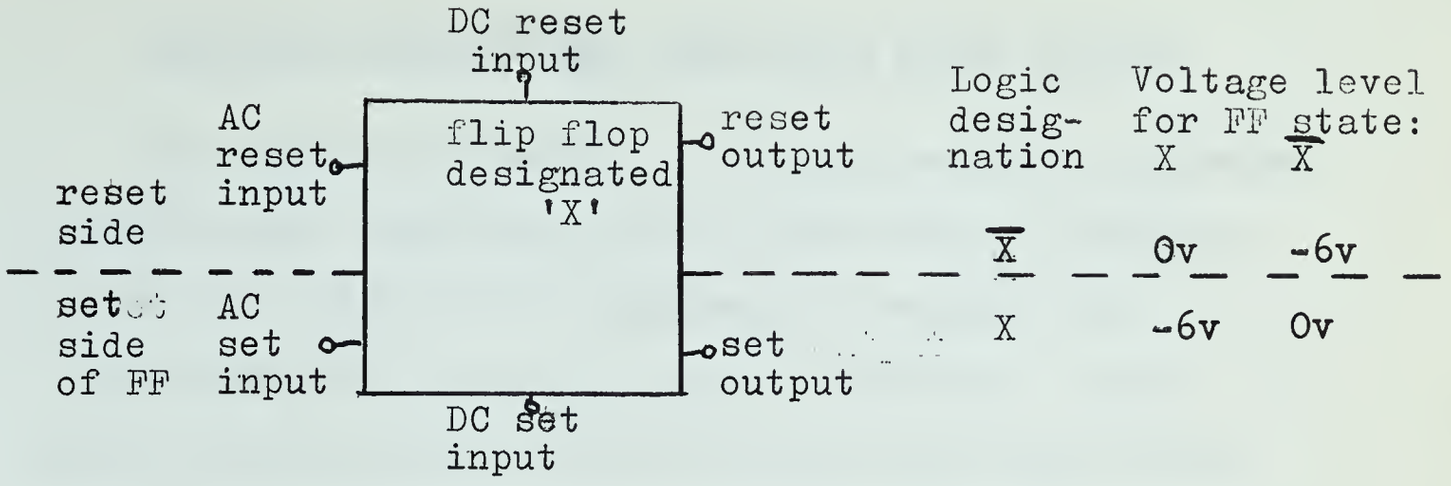


FIGURE 9 FLIP FLOP NOTATION

DIVIDE BY 100 COUNTER

The counter consists of seven B8 920 00 Philips flip flop building blocks connected in series. Feedback from the last one to the 16, 8, and 4 stages reduces the count from 128 to 100. A resetting voltage to insure that all the flip flops start in the same state is fed through resistors and isolating diodes from a momentary contact to the -6 volt supply after the unit has been turned on. This same pulse resets all the other flip flops in the unit as well.

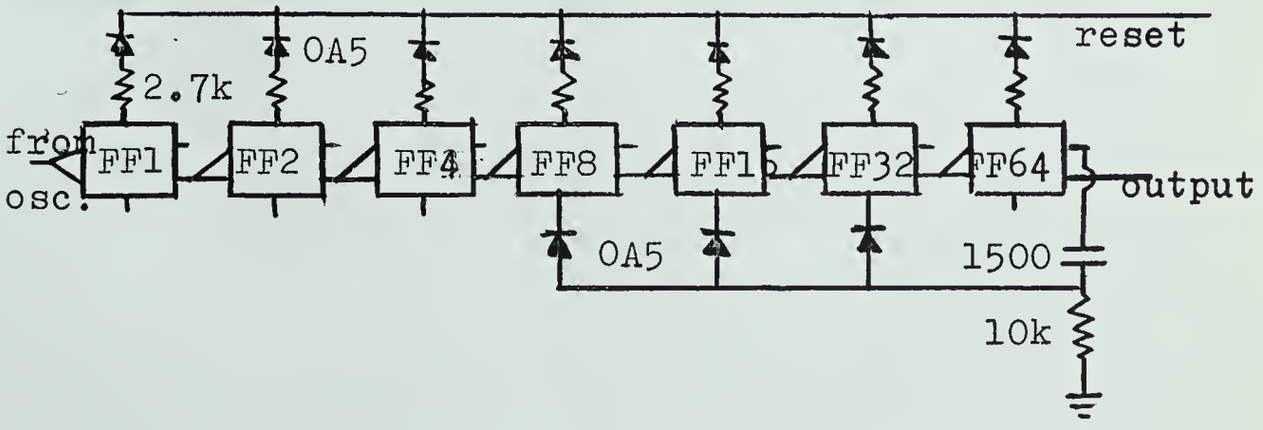
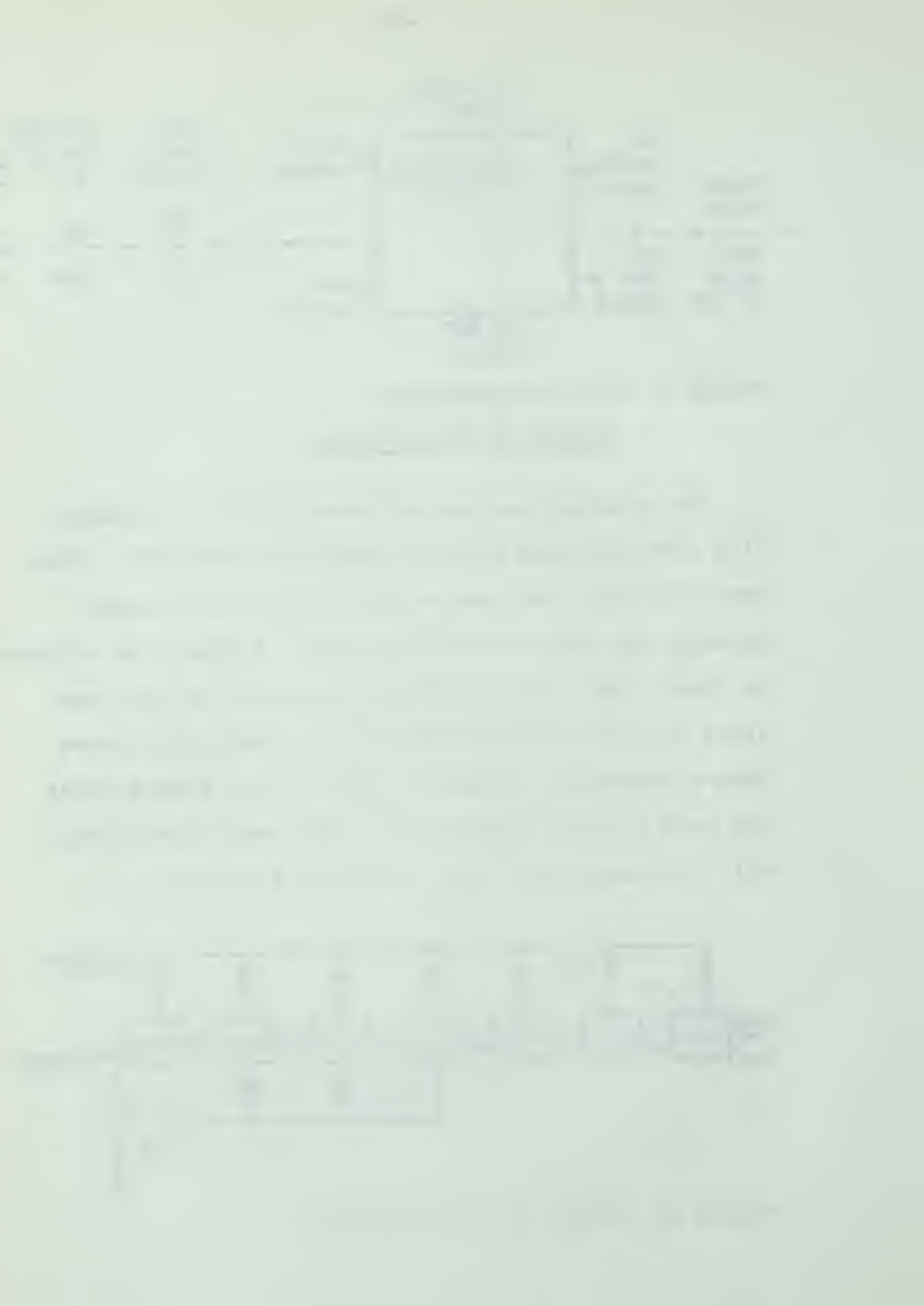


FIGURE 10 DIVIDE BY 100 COUNTER.



SQUARING INVERTER AND CONVERSION DELAY STAGES

The squaring inverter is a simple single transistor switch which supplies a square pulse with a negative going rise time of 0.1 microsecond, required for triggering the analog to digital converter. Since the Philips monostable multivibrator building blocks have a low input impedance an isolating inverter must be inserted to reduce loading on the squaring inverter and to obtain the correct polarity of pulse to trigger the monostable. A Philips building block inverter was found adequate for this purpose.

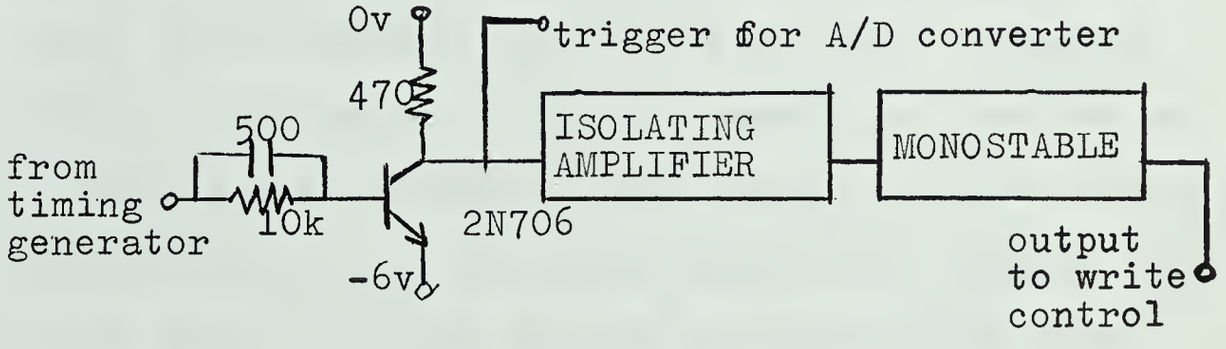


FIGURE 11 SQUARING INVERTER AND CONVERSION DELAY

LINE SELECTION CONTROL

The heart of the line selector consists of four Philips flip flop blocks connected in series with feed back so as to count by ten. The input pulse, which changes the states of the flip flops, also triggers two monostable multivibrators in series, each with about a three microsecond period. The first allows the relatively slow flip flops to attain their full logic voltages, and the second produces a strobing pulse to ensure that the outputs occur simultaneously.

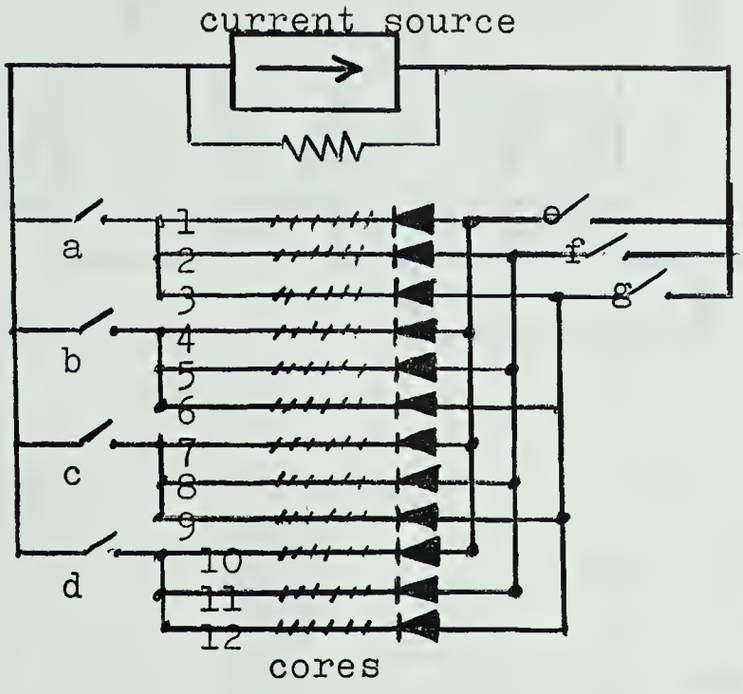
One method of selecting the core line to be driven from the flip flops is to use one selection gate for each line. These must be 3, 4, and 5 input gates, (logic plus strobe inputs) and each uses a separate switch. This method is fairly waseful of components. By letting the switches themselves also act as gates, seven switches (and the seven gates that trigger them) can be used to select any one of twelve core lines, as shown in Figure 12. This is a 40% saving in switches and gates over the previous method. There are only ten core lines in this particular design, but the seven switches are still a minimum. The logic to drive these switches from a standard count by ten flip flop arrangement becomes quite complicated as

shown in Figure 14.

In search of a simpler system of gates, it is evident from the logic in Figure 12, that a divide by three counter gated to produce e, f, and g, followed by a divide by four counter gated to produce a, b, c, and d is all that is needed. These will be two input gates (three with the strobing pulse) of a much simpler nature than before. It is also necessary to reduce the count of the suggested dividers from 12 to ten for the matrix to be used. A A divide by three counter is easily obtained from a divide by four arrangement by simple feedback. This changes the logic count as shown by Figure 15.

To achieve the shorter count required by the logic of Figure 13, counts 13 and 14 of Figure 15 must be skipped. A gate from DC selects step 13 and sets A and B to correspond to step 16, and the required counts are skipped. The gate logic, as shown in Figure 15 is much simpler than that shown in Figure 14.

The switches, as shown in Figures 12 and 13, allow the ten lines to be cycled through sequentially. A gate selects the tenth core line combination, and uses it to step the Y counter. The Y counter does not have the strobe pulse generator, but uses the strobe pulse from the X counter in its gates. The



To select core line	close switches
1	a and e
2	a and f
3	a and g
4	b and e
5	b and f
6	b and g
7	c and e
8	c and f
9	c and g
10	d and e
11	d and f
12	d and g

FIGURE 12 MINIMUM SWITCHING ARRANGEMENT FOR 12 LINES

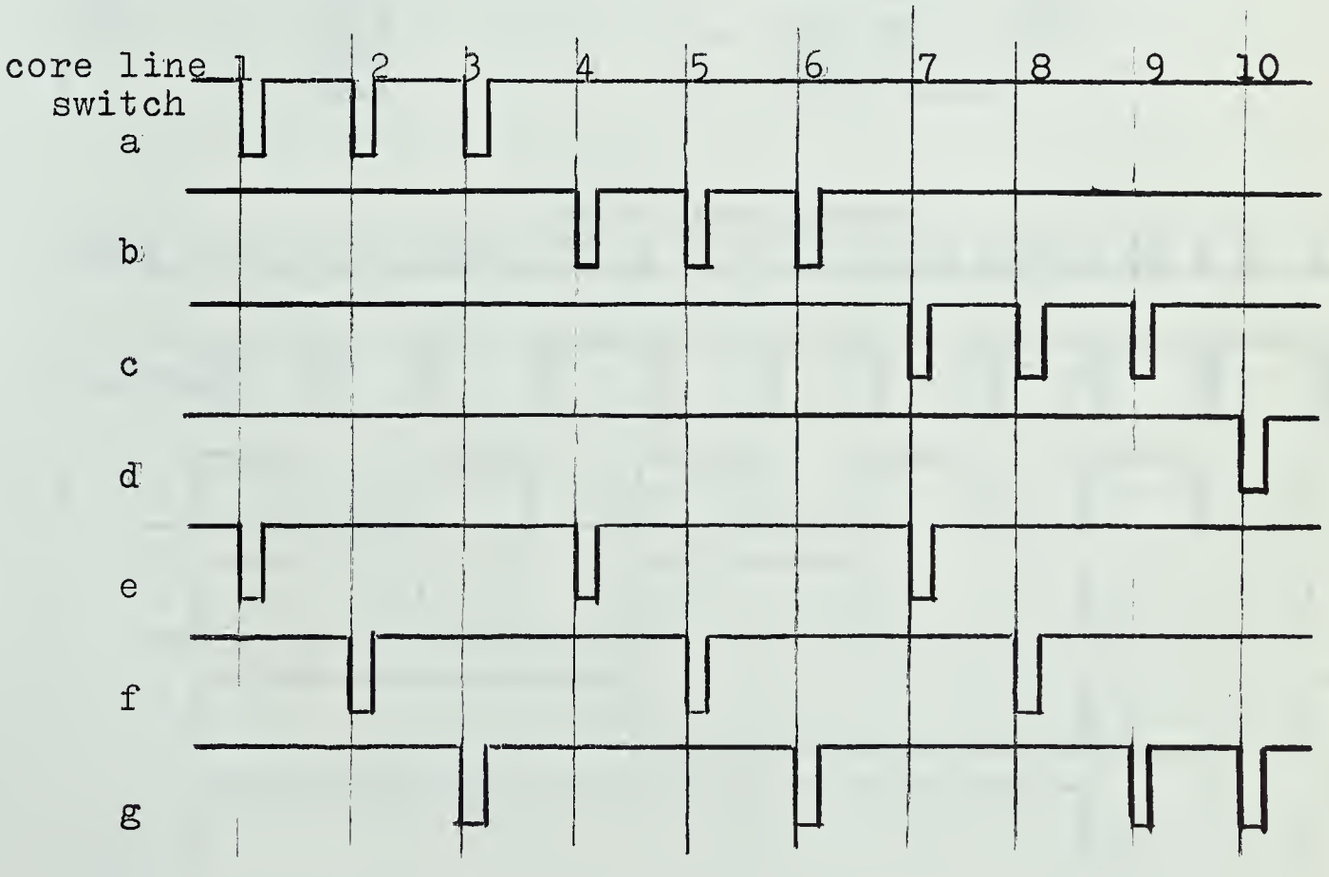
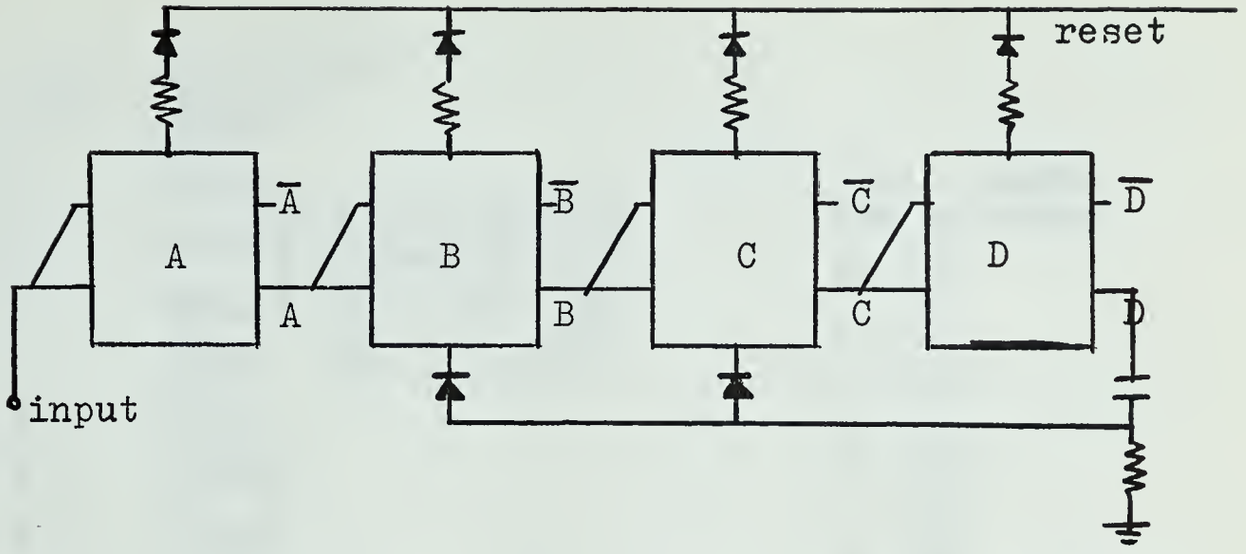


FIGURE 13 PULSE SEQUENCE NECESSARY FOR THE SEVEN SWITCHES TO SELECT ONE OF TEN CORE LINES



logic steps	flip flop state
I	$\bar{D}\bar{C}\bar{B}\bar{A}$
II	$\bar{D}\bar{C}\bar{B}A$
III	$\bar{D}\bar{C}B\bar{A}$
IV	$\bar{D}\bar{C}BA$
V	$\bar{D}C\bar{B}\bar{A}$
VI	$\bar{D}C\bar{B}A$
VII	$\bar{D}CB\bar{A}$
VIII	$\bar{D}CBA$
IX	$DCB\bar{A}$
X	DCBA

logic needed for switches

a= $(\bar{B}\bar{C}\bar{D}+\bar{A}\bar{C}\bar{D})t$

b= $(\bar{B}\bar{C}\bar{D}+AB\bar{C}\bar{D})t$

c= $(ABC+BC\bar{D})t$

d= $(\bar{A}BD)t$

e= $(\bar{A}\bar{B}\bar{C}+AB\bar{C}+\bar{A}BC\bar{D})t$

f= $(A\bar{B}\bar{C}+\bar{A}\bar{B}C+ABC\bar{D})t$

g= $(\bar{A}B\bar{C}+A\bar{B}C+D)t$

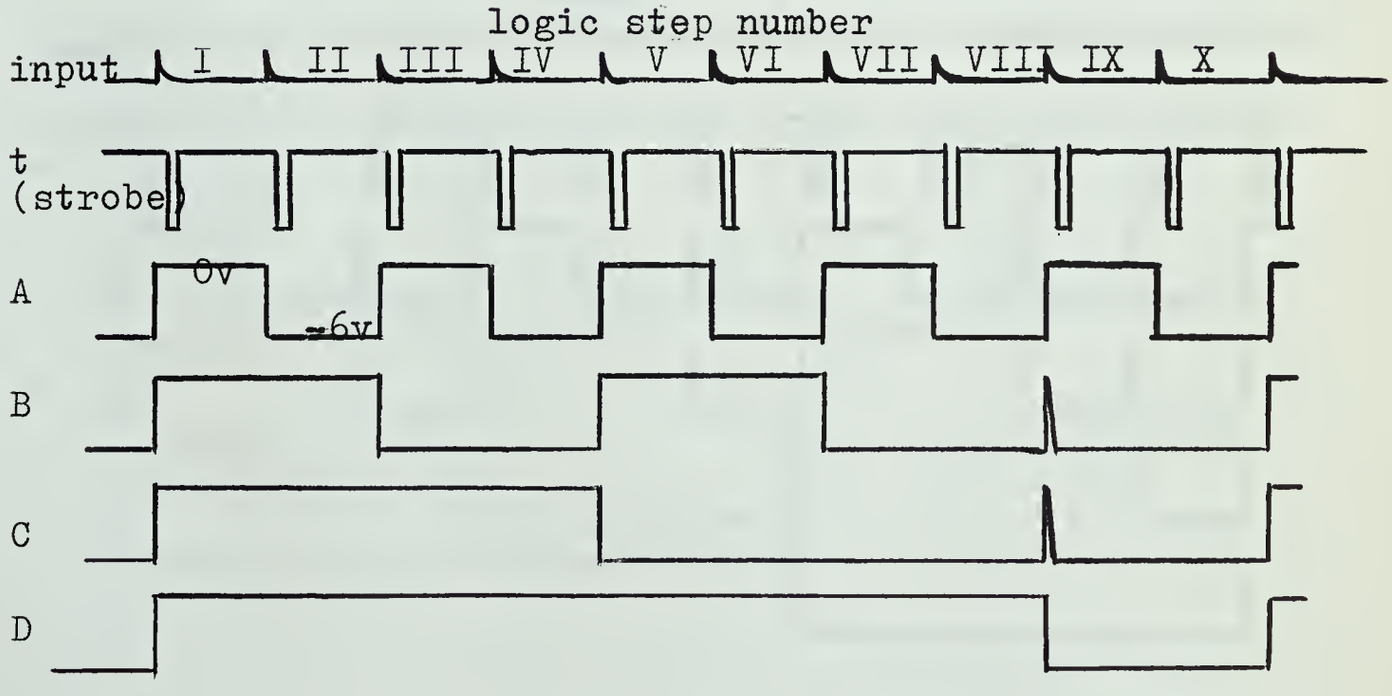


FIGURE 14 LOGIC ARISING FROM A CONVENTIONAL FLIP FLOP CONNECTION

count	flip flop states
1	$\bar{D}\bar{C}\bar{B}\bar{A}$
2	$\bar{D}\bar{C}\bar{B}A$
3	$\bar{D}\bar{C}B\bar{A}$
4	$\bar{D}\bar{C}BA$
5	$\bar{D}C\bar{B}\bar{A}$
6	$\bar{D}C\bar{B}A$
7	$\bar{D}CB\bar{A}$
8	$\bar{D}CBA$
9	$D\bar{C}\bar{B}\bar{A}$
10	$D\bar{C}\bar{B}A$
11	$D\bar{C}B\bar{A}$
12	$D\bar{C}BA$
13	$DC\bar{B}\bar{A}$
14	$DC\bar{B}A$
15	$DCB\bar{A}$
16	$DCBA$

$\bar{B}$ changing to B sets $\bar{A}$ to A so counts of 3, 7, 11, 15, are skipped.

$D\bar{C}$ changing to DC sets $\bar{B}\bar{A}$ to BA so counts of 13, 14, 15, are skipped

logic needed for switches

a= $\bar{C}\bar{D}t$

b= $C\bar{D}t$

c= $\bar{C}Dt$

d= CDt

e= $\bar{A}\bar{B}t$

f= $A\bar{B}t$

g= ABt

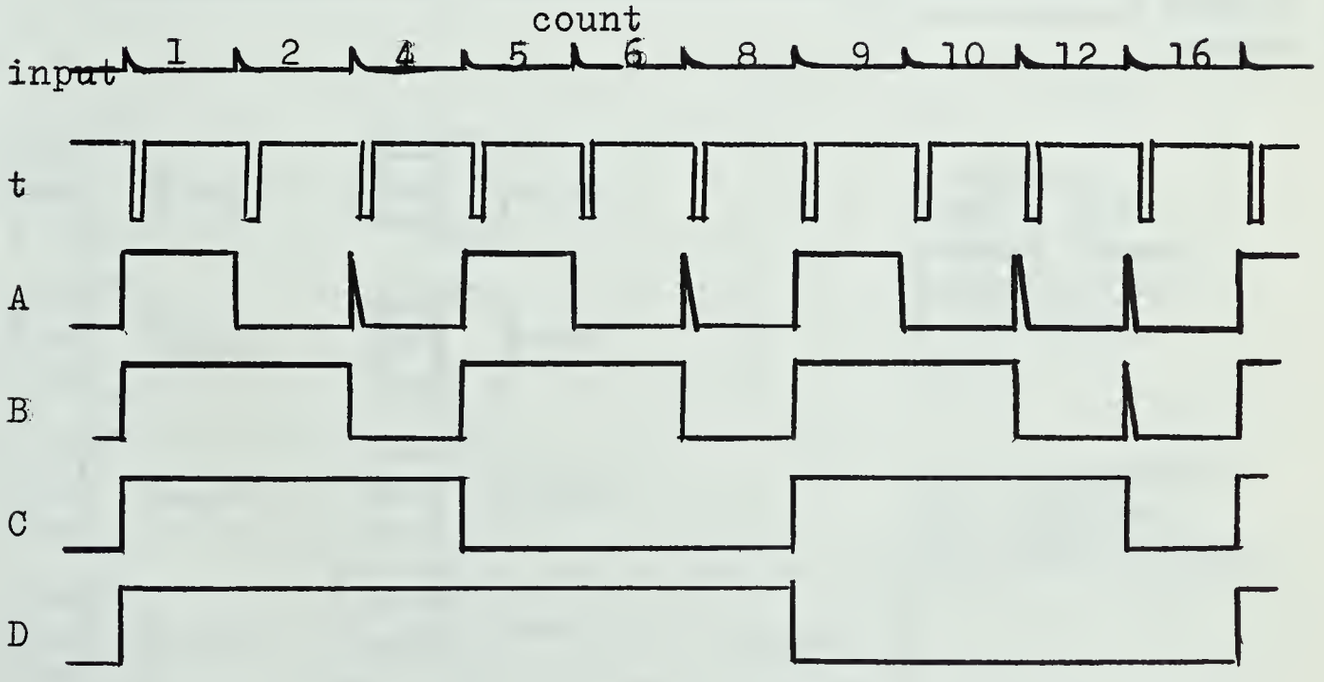


FIGURE 15 SEQUENCE OF OPERATIONS OF SPECIAL COUNTER ARRANGEMENT

combined X and Y switching allows the whole hundred cores to be cycled through in order, and to continue in that fashion. A complete diagram of a single control is shown in Figure 16.

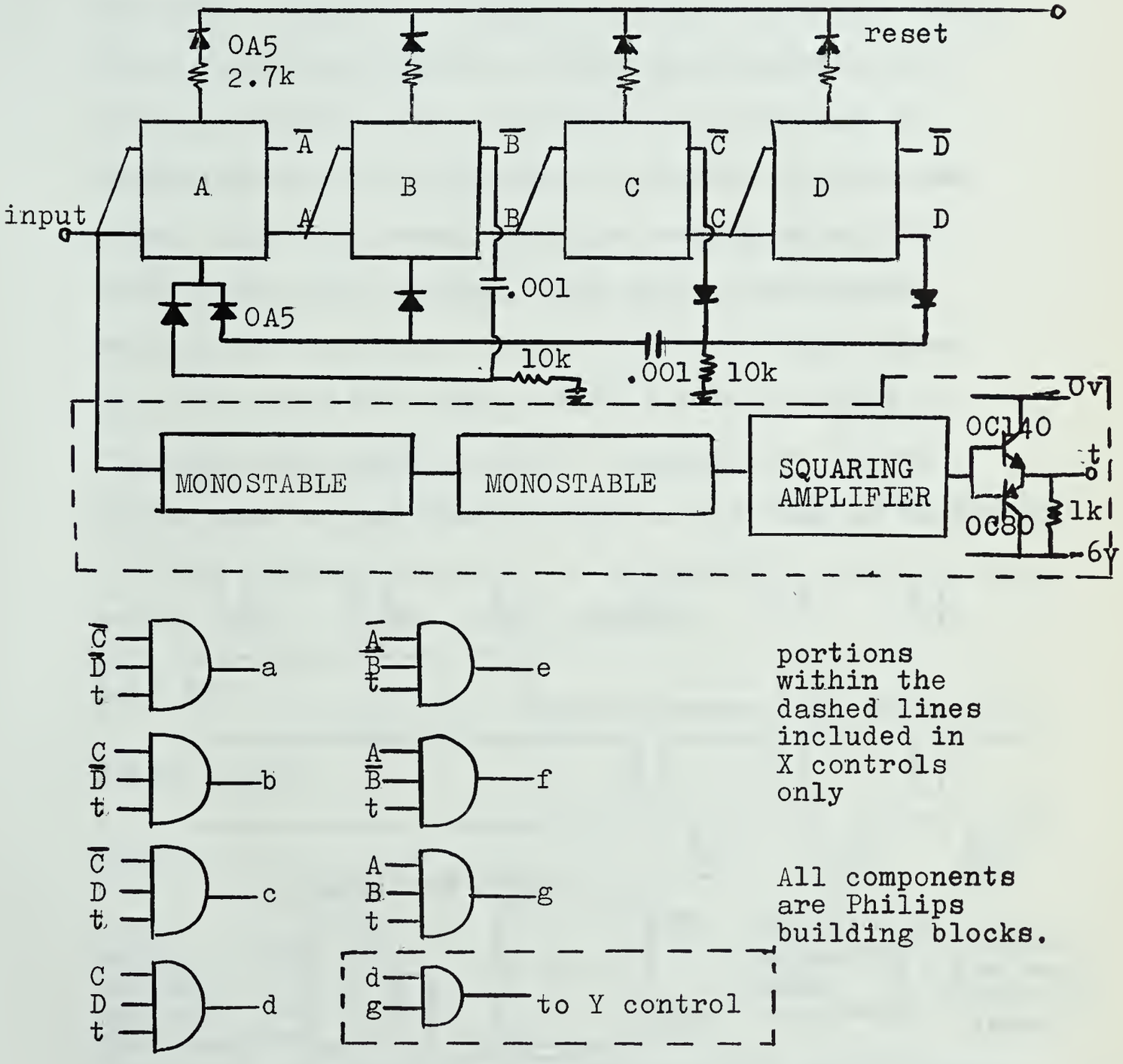


FIGURE 16 COMPLETE LINE CONTROL CIRCUIT

DELAY CONTROL (FIGURE 17)

The signal which writes the 99th core is selected by a gate and sets the flip flop. This holds the second gate open, allowing the strobe pulses from the write control to trigger the read control. Since it is starting from zero, while the hundredth core is being written, the information is read out one cycle before new information is written in the same core.. This continues, with the reading being 100 cores behind the writing, thus giving the maximum resolution for a given delay. Shorter delay times than 100 times the clock period can be obtained by starting the readout sooner. Changing the inputs to the gate to any desired core is all that is necessary.

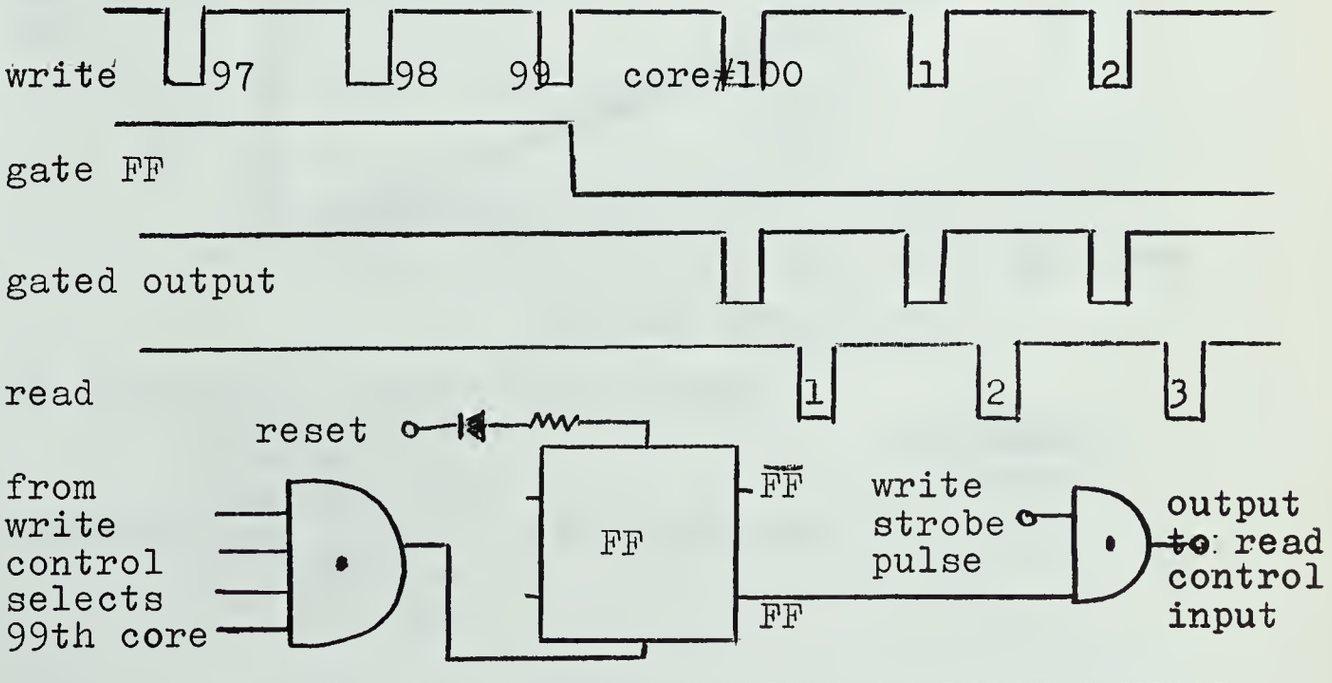
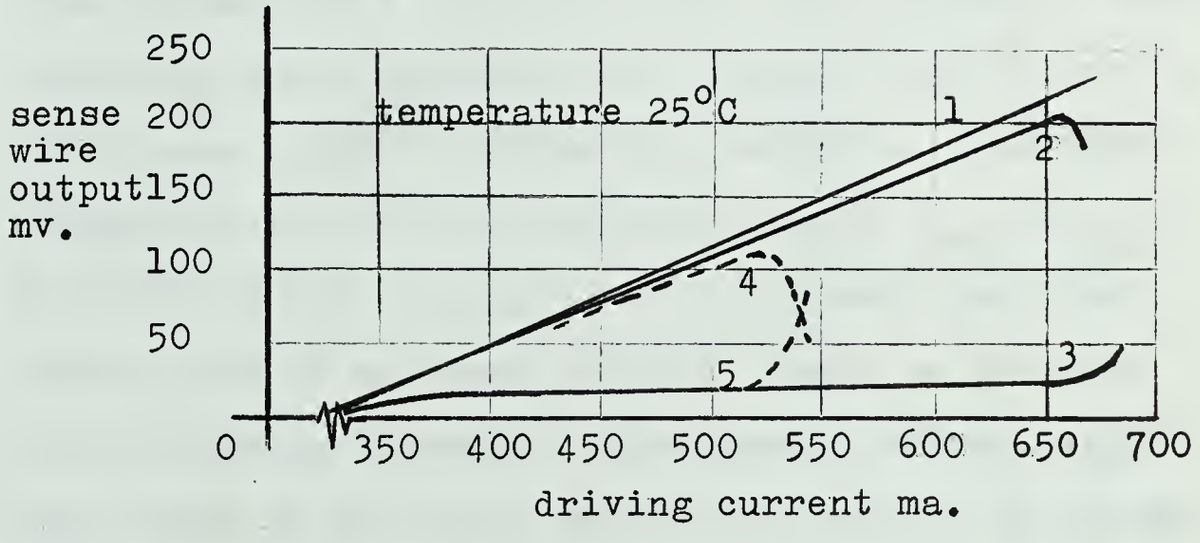


FIGURE 17 OPERATION AND CONSTRUCTION OF DELAY CONTROL

CORE SWITCHES

The chart of core characteristics (Figure 18) provided by the manufacturer shows that no output voltage can be expected from a core with driving currents smaller than 325 ma., i.e., this is the minimum current that will cause a change of state. As the driving current is increased the size of the hysteresis loop is increased and the larger flux change produces a larger output, as shown by curve 1 in Figure 18. It would seem desirable then, to have the driving currents as large as possible.



d= disturbance ratio = 0.5 (ideal)
1 undisturbed one
2 disturbed one
3 disturbed zero
d=disturbance ratio = 0.6 (10% error)
4 disturbed one
5 disturbed zero

$$d=\frac{I_{half}}{I_{full}}$$

FIGURE 18 SENSE WIRE OUTPUT VERSUS DRIVING CURRENT

There is a limit, however, as shown by curves 2 and 3. These represent outputs from disturbed cores, ones that have had half the total switching current driven through them when another core was addressed on a previous cycle. This half current has been enough to change the strength of the remenant magnetization such that the outputs, when they are read, tend to become ambiguous, i.e., the half currents are large enough to partly switch the cores.

If the switching currents are not equal, i.e., through errors the half switching currents are not exactly half the total current chosen, these ambiguous outputs will occur at lower drive levels. This effect is shown in Figure 18, curves 4 and 5, for a worst case error of 10% in the currents. The disturbance ratio in this case would be $d = I_{half}/I_{full} =$ 0.5+10%/1.0-10% = 0.55/0.9= 0.6. It was found that better than 5% accuracy (d=0.55) could be achieved in the driving currents, consequently 600 ma. ($\pm$5%) was chosen as the total switching current, or 300 ma ($\pm$5%) as the half switching current.

Core switches were needed which would drive currents in both directions through the core lines. There were two basic types used, as shown in Figure 19. The driver stage is a saturated switch which changes

the 0 volt and -6 volt input levels to -6 volt and +6 volt respectively. These levels drive saturated switches which may be either in the common collector configuration or in the common emitter configuration.

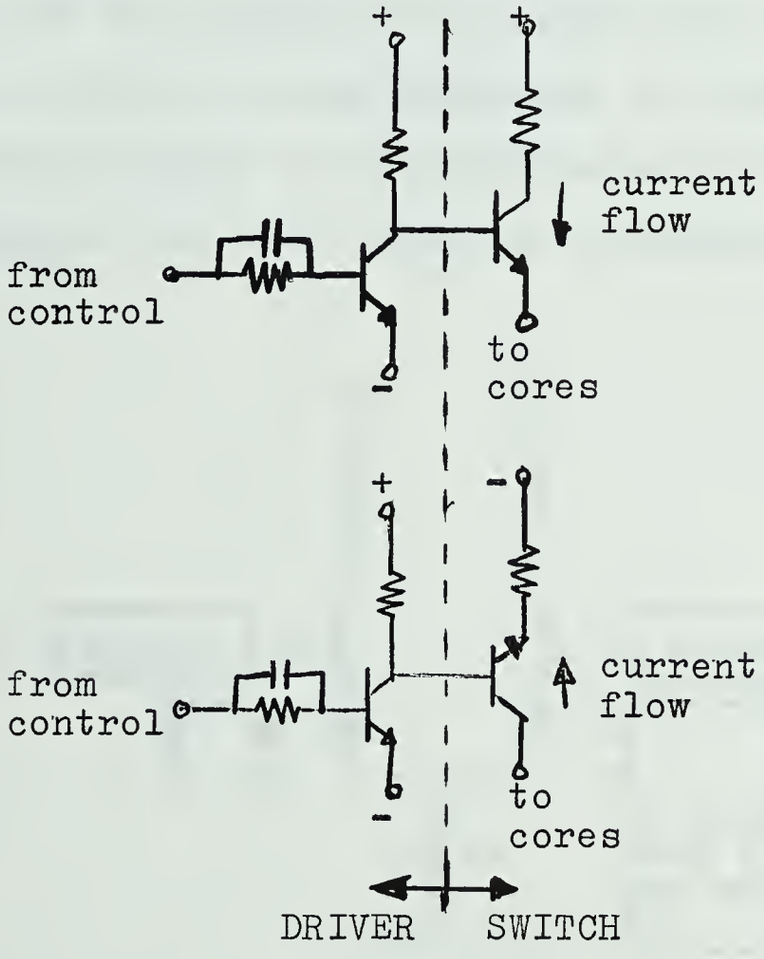


FIGURE 19 BASIC CORE SWITCHES

In this fashion current is driven in both directions using a very similar basic circuit. The switches are connected in groups as shown in Figure 20. The left pair of switches A and B, when both turned on, will drive current in one direction, and the right pair in the other direction through the core line.

Read and write directions are decided arbitrarily. Only the one set of switches and one core line is shown. Others are connected after the fashion of Figure 12, which is shown for one current direction only. The two directions are connected to the core lines via the diodes as indicated in Figure 20. The diodes isolate the lines from each other and also isolate the write from the read switches on any line.

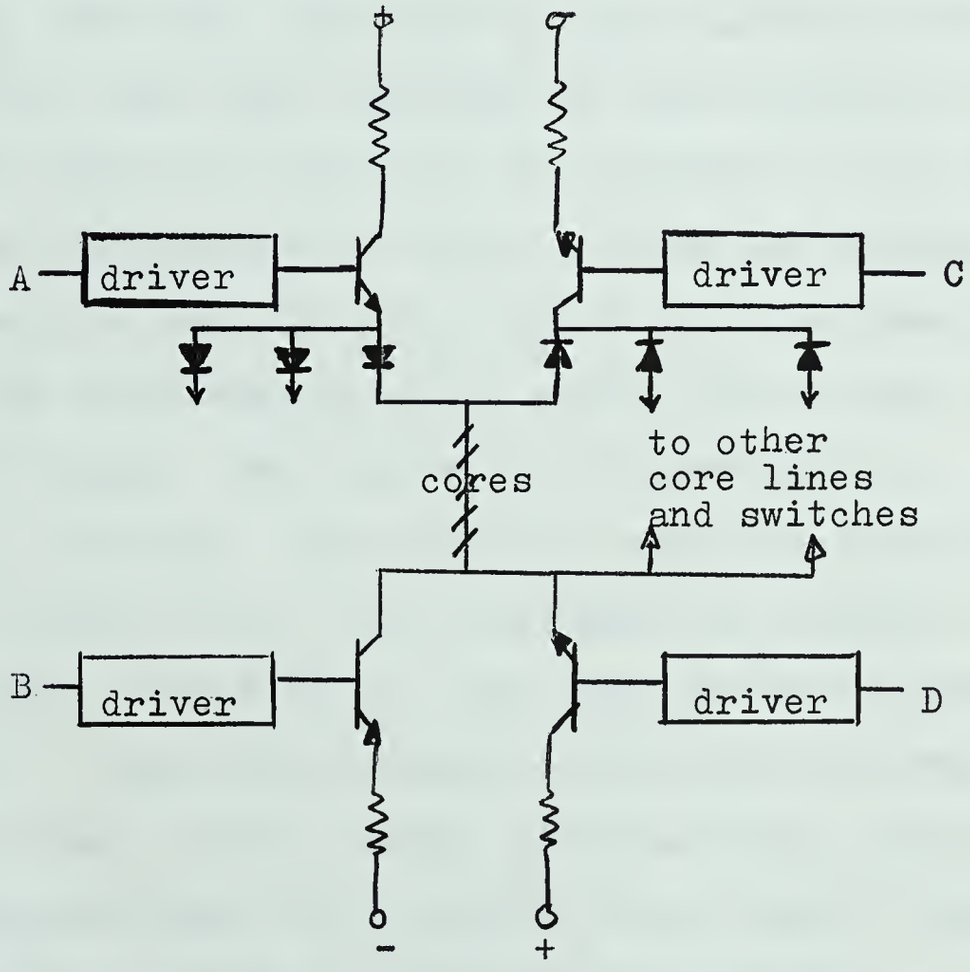


FIGURE 20 ARRANGEMENT OF READ AND WRITE SWITCHES

The switches are always turned on in pairs, a top along with a corresponding bottom one, so there never exists the problem of trying to drive current through an open switch. The current source consists of the two saturated transistors, the foreward biased diode, and the two load resistors across the positive to negative supply lines. Load resistors of 18 ohms for each switch supply the 300 ma. half switching current required. When both switches on one side are on, the core line rests at about ground potential. This will mean that the bases of the switching transistors (and the collectors of the drivers) will be held at approximately 0 volts. Since the transistors driving the bases are off, this 6 volt drop must come from the base current of the switch through the load of the driver. Base current of the switch is I_c/h_{fe} = 5.5 ma. Thus for the 6 volt drop the driver load is set at 1k. This driver must be saturated when the input is at 0 volt. This sets the base resistor at 47k. A capacitor is needed across this to sweep out the base stored charge, given as being typically 720 microcoulombs for a 2N1306, hence C=Q/V = 120pf. A 100 pf capacitor was found to be adequate.

DIGIT INHIBIT SWITCHES

The same switches were used for digit inhibit switches, except, after running through the core, the line was grounded instead of going to another switch. The switches are turned on by gates connected to the analog to digital converter outputs and to the write strobe pulse.

READOUT SYSTEMS

The voltage output produced on the sense line by a core that switches is about 120 mv. The voltage produced by cores which do not switch, but are disturbed add to about 10 mv. Switching transients which are picked up by the sense windings from the drive and inhibit wires may be as high as 50 mv. but are of a much shorter duration than the core outputs. The typical output of a sense winding is shown in Figure 21.

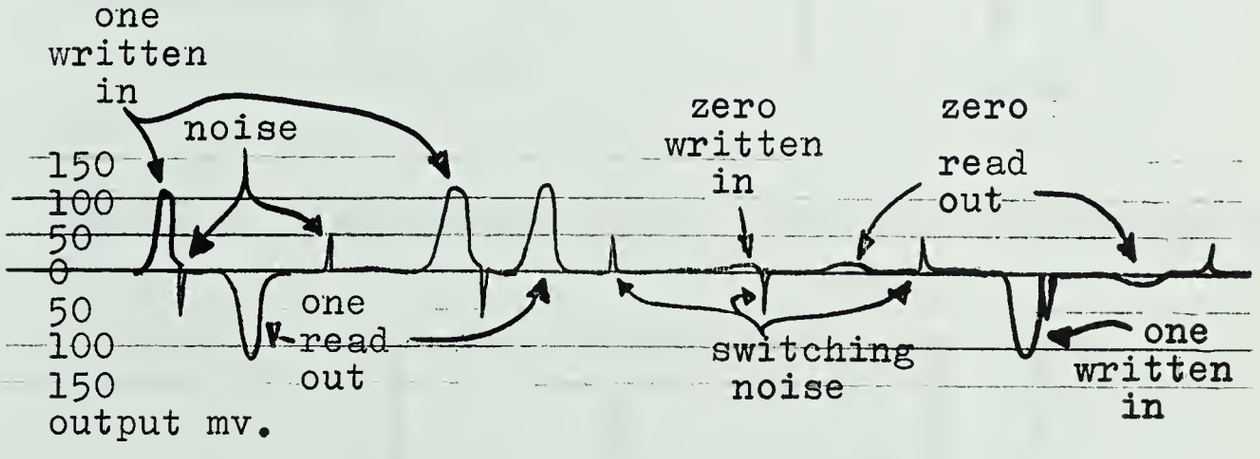


FIGURE 21 TYPICAL OUTPUT OF A SENSE WINDING

The desired output pulses may be either positive or negative going. Pulses arising from the writing in of information may also go in either direction. These must be removed from the final output, along with the noise spikes.

The type of readout used in large commercial computers,[4] shown in Figure 22, has a push pull amplifier for the input stage. The output of this is coupled via a transformer to a voltage doubler and emitter follower. This signal is gated with a strobe pulse to remove the write signal and switching

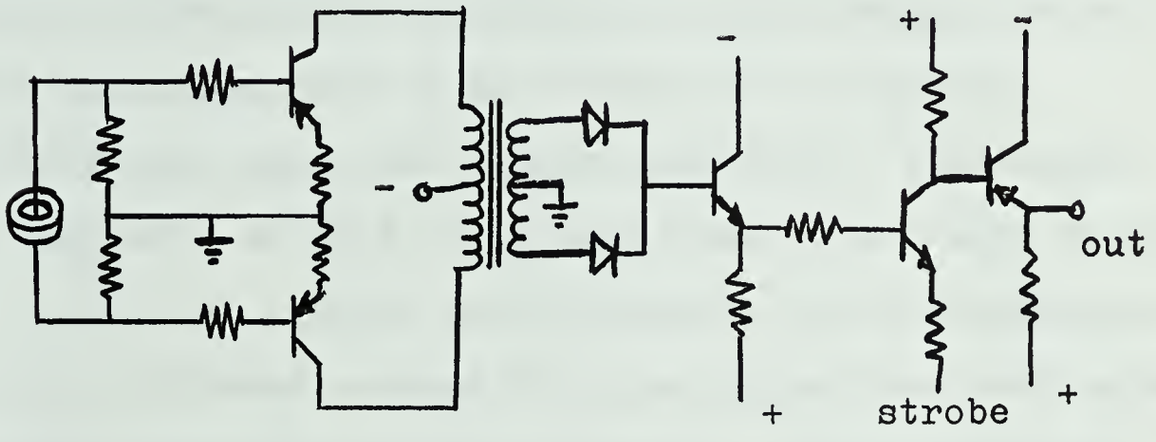


FIGURE 22 SIMPLIFIED READOUT CIRCUIT OF IBM7090 COMPUTER

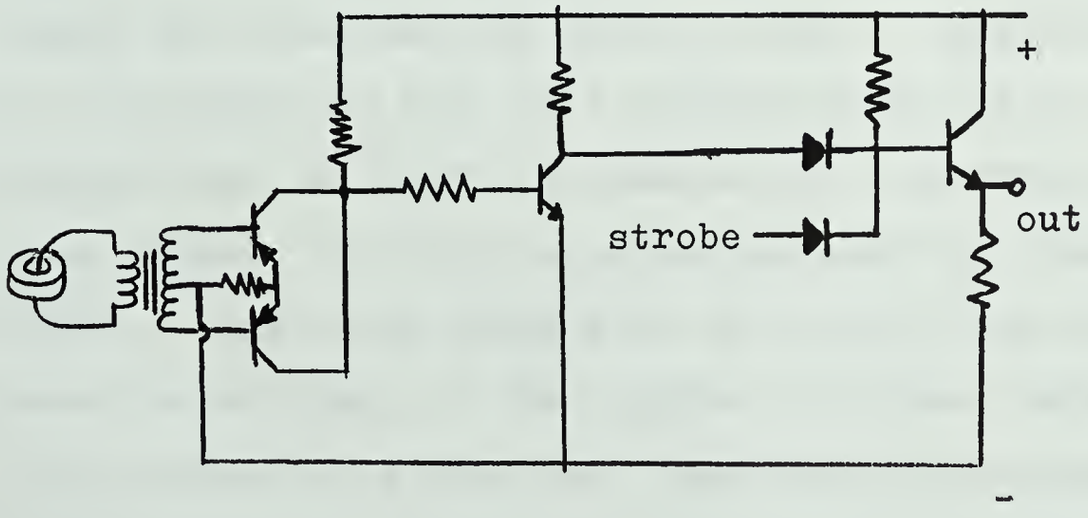


FIGURE 23 LESS COMPLICATED READOUT CIRCUIT

noise, and fed through an isolation stage to the output. Since there must be one of these amplifiers for each output bit, this method can become quite expensive. A less sophisticated system, [5] Figure 23, which can be used on smaller matrices such as this one, consists of a transformer coupled push pull amplifier with a common collector resistor which essentially rectifies the input signal as well as amplifying it. It is followed by a squaring amplifier, gate, and buffer amplifier. This system eliminates several components, but it is still expensive.

An even simpler system consists of a differentiator which produces a negative going spike from each input pulse regardless of its polarity. A two transistor amplifier will bring this up to the logic voltage where it can be gated with the read select pulse to remove the noise and and write pulses. A drawback of this system is that on a negative going input the leading edge is amplified, whereas on a positive going sense output, the trailing edge produces the final output. This means there will be a one to two microsecond uncertainty in the outputs. For most computer applications it is desirable that the outputs appear simultaneously. It is particularly necessary in this application since all the reference flip flops must

in the digital to analog converter must change states at the same time to minimize switching transients. If the output pulses of the amplifiers are used to set flip flops, and the outputs of these flip flops gated with a strobing pulse, the gated outputs will be simultaneous. This also greatly reduces the requirements on the shape of the amplifier output, eliminating the need for the squaring amplifier and buffer. The outputs will be held for the major portion of the cycle, and could be sampled several time if necessary, which could not have been done with other systems. The flip flop can be reset by the write pulse in preparation for the next read cycle. This scheme still uses the same number of transistors, four per readout, but eliminates costly transformers. There is the additional cost of producing the strobing pulse, however. In this unit a clock pulse must be generated for the digital to analog converter and this pulse will serve, so no additional components are needed. The only disadvantage to this readout system is that the information is not available until the strobing pulse occurs, rather than when the cores switch, a delay of about two microseconds. This is no real disadvantage in this system, but could be intolerable in faster systems. Figure 7 includes

the pulse time relationships of the outputs.

The approximate shape of the output pulse and its derivative is shown in Figure 24. The pulse is differentiated by the coupling capacitor and the input impedance of the first stage. The transistor

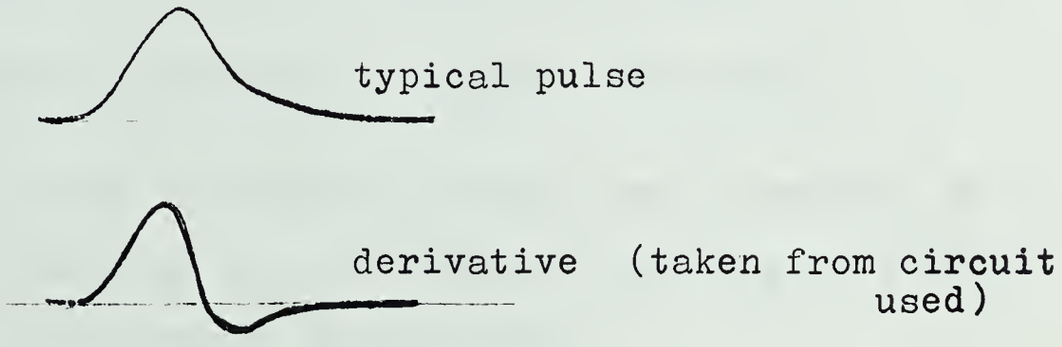


FIGURE 24 SENSE LINE OUTPUT PULSE AND ITS DERIVATIVE

is biased on the verge of saturation, so that a negative going pulse will be amplified, but a positive going one will drive it further into saturation and will produce no output. The second stage is similar, except that it uses a complementary transistor and is operated further into saturation. The output is gated with the read select pulse to remove unwanted outputs. The selected output is used to set a Philips building block flip flop. It is reset by the write pulse in preparation for the next output. The complete amplifier is shown in Figure 25. The input is connected between the base and emitter of

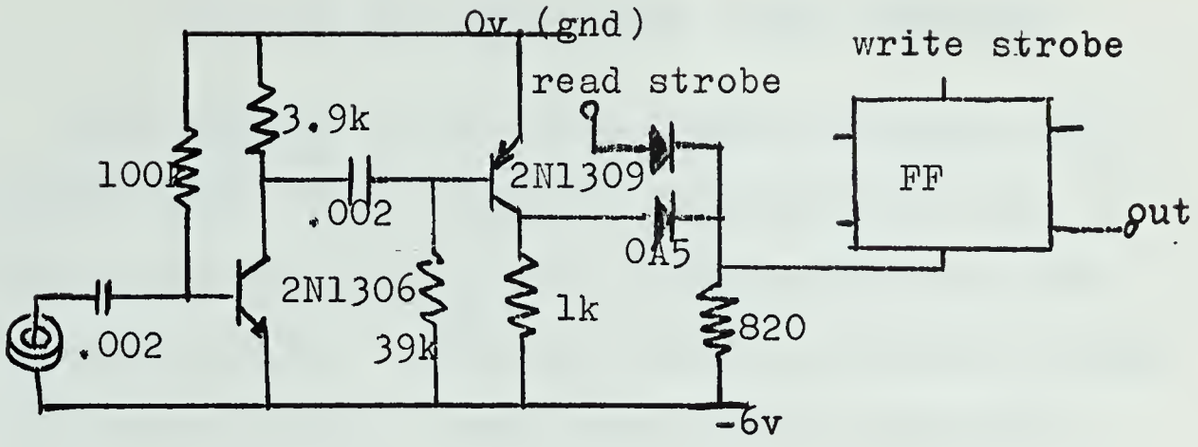


FIGURE 25 CIRCUIT OF READOUT AMPLIFIER

the first transistor rather than to ground, so as to minimize spurious pulses resulting from noise on the negative supply line.

DIGITAL TO ANALOG CLOCK PULSE GENERATOR

The digital to analog converter requires clock pulses that are at least 0.6 microseconds wide, of both positive and negative polarity, and with six volts amplitude. This pulse must be included within the limits of the input pulse to the converter. With the flip flop holding, this reduces to a short pulse after the flip flops have been set. This is achieved as shown in Figure 26, by triggering a monostable multivibrator from the write strobe pulse. Its period is adjusted so that it changes state again just after the readout pulse sets the flip flops, as in Figure 7. The monostable multivibrator output is differentiated, and the resulting negative going spike amplified by two Philips inverting amplifiers. The negative pulse resulting from the second of these is one microsecond wide, which is adequate for the negative clock pulse. It is coupled to a saturated switch operating between the positive supply line and ground, which yeilds the corresponding positive pulse required.

POWER SUPPLY FILTERING

The logic section draws about 800 ma from the negative supply, and about 100 ma from the positive supply. When all ones are being written in the cores, or during readout, an additional 600 ma is needed from each. When zeros are being written in all the digits of the memory, about 4 amps is needed for the switching. This current is roughly divided between the supplies. These high currents are being drawn in the form of fairly short pulses, and this places considerable stress on the power supply regulators. The supplies being used, three amp modular units, showed a tendency to ring, or even oscillate violently under some conditions of switching. Paper and electrolytic capacitors across the lines stopped this, but left switching transients of about 0.5 volts. This does not interfere appreciably with the action of the switches, but it is not allowable in the logic section. A set of LC filters in the supply lines to the logic cut the spikes to less than 0.05 volt, which is quite acceptable. Figure 27 shows the final form of filtering used.

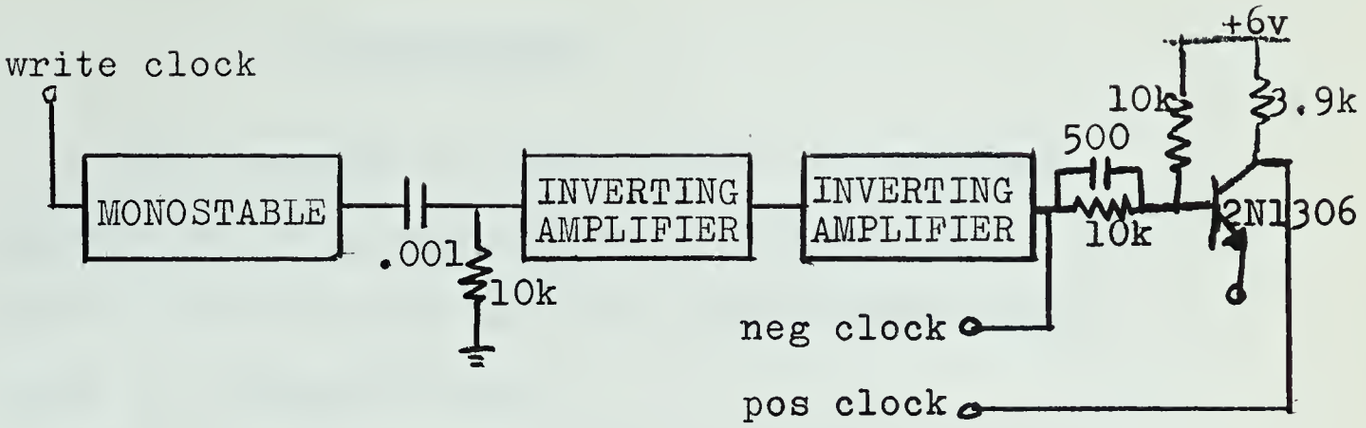


FIGURE 26 DIGITAL TO ANALOG CONVERTER CLOCK PULSE GENERATOR

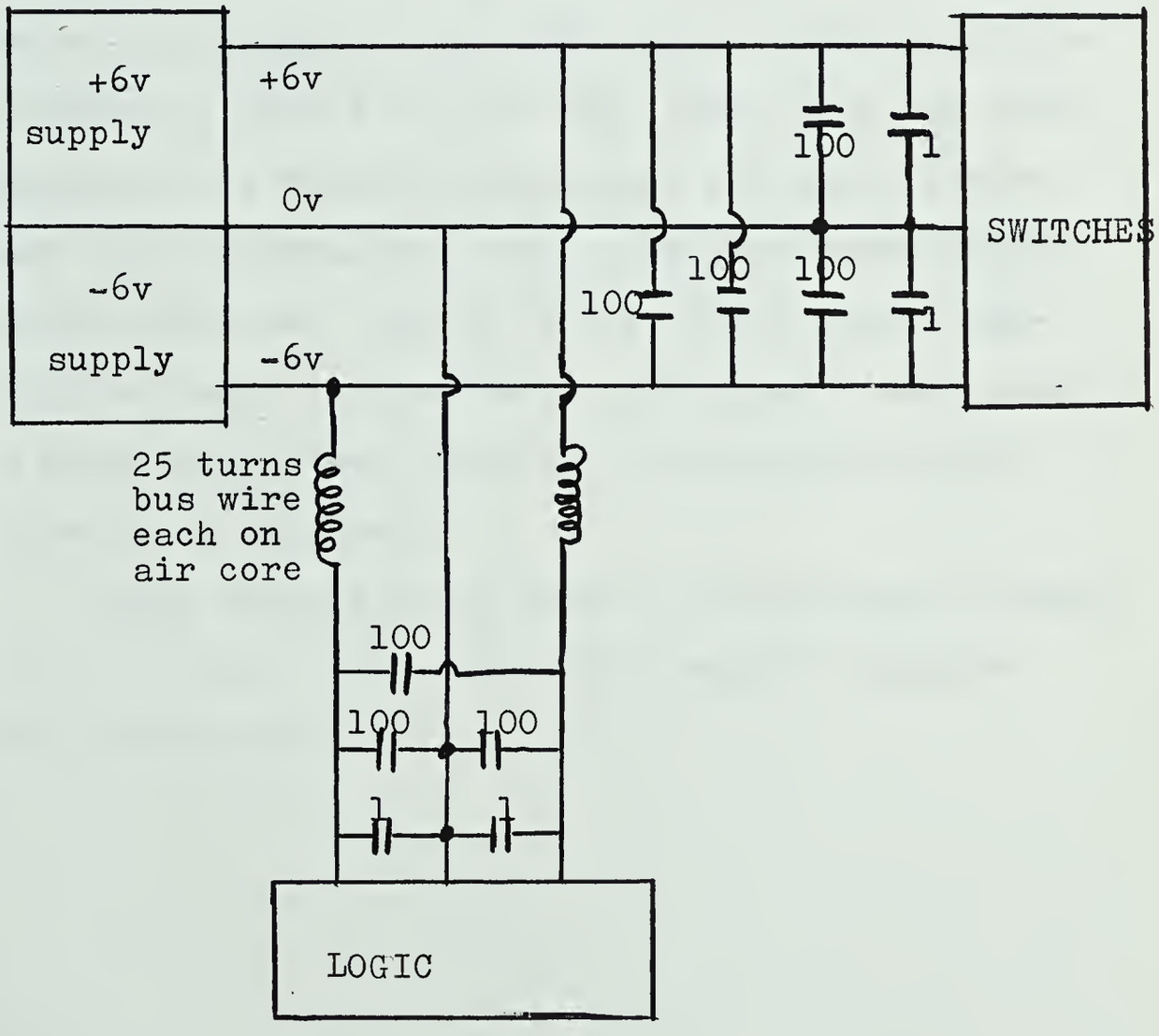


FIGURE 27 POWER SUPPLY FILTERING

CONCLUSIONS

The objective of constructing the required memory and delay was achieved. Although the unit is fast enough as it is, improvements could lead to increased speed.

Use of faster logic blocks than the present Philips units would be necessary. Micro circuits might serve the purpose well. All logic levels should be clamped by diodes to a voltage lower than the power supply. This would not only make the logic faster and more uniform, but would eliminate power supply noise problems. Faster, better power supply regulation could be considered. With the faster logic, a more conventional type of readout system would have to be employed.

These changes would lead to an increase in speed of up to five times, but would require complete reconstruction.

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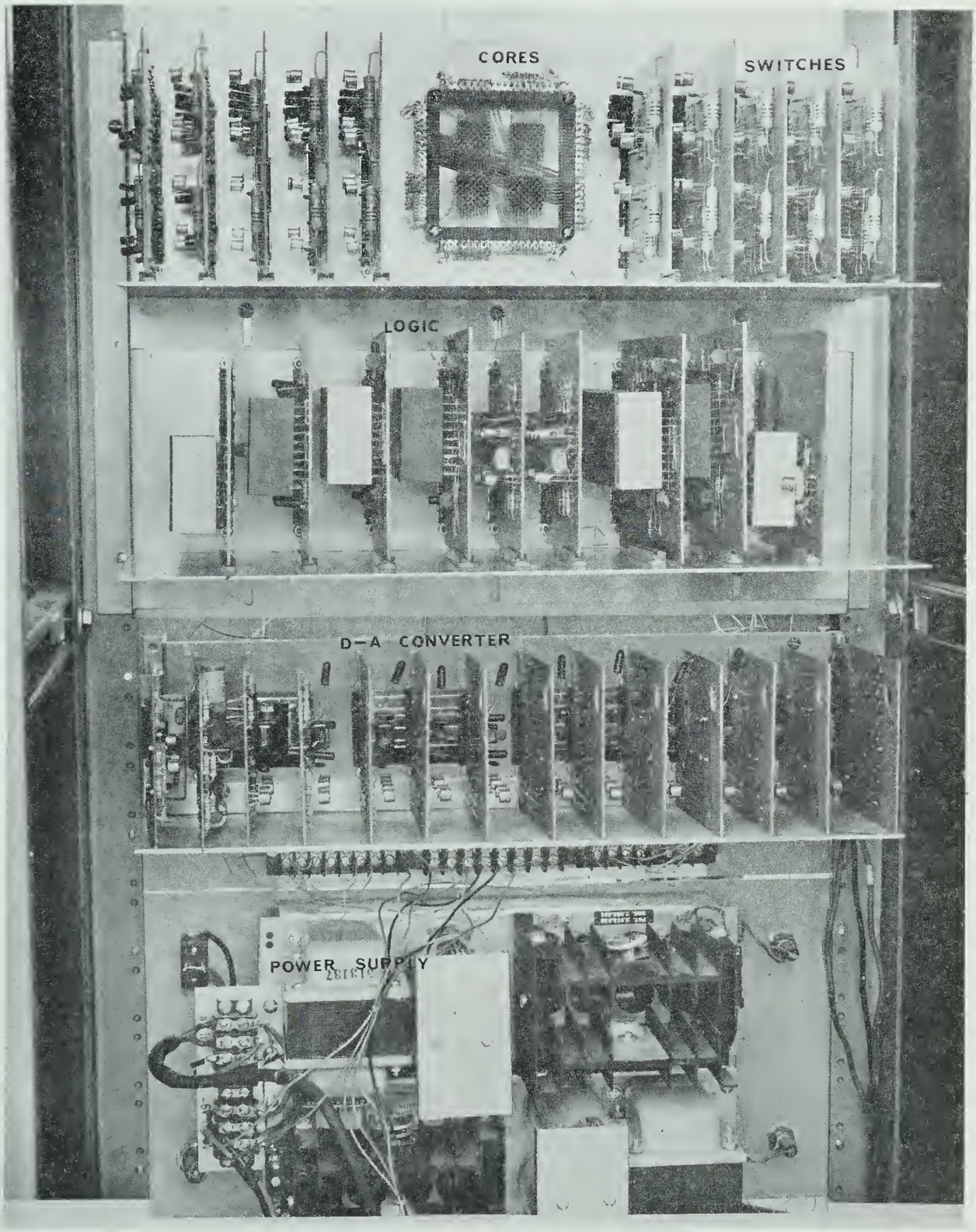

FIGURE 28 PHOTOGRAPH OF THE MEMORY AND DIGITAL TO ANALOG CONVERTER